UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,620	08/07/2001	Marcus Tong	2001P4227US01	3155

7590 05/17/2006

Siemens Corporation
Attn: Elsa Keller, Legal Administrator
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
CHANG, RICHARD	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,620	TONG ET AL.	
	Examiner	Art Unit	
	Richard Chang	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/09/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10, 12, 14, 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments, filed on 03/09/2006, with respect to claims 1-10, 12, 14, and 16-20 have been fully considered but they are not persuasive. Examiner does not withdraw the obviousness rejection to Paradine et al. in view of Hirata. Please refer to the response to argument section for the detailed explanations.

Claims 11, 13 and 15-18 had been canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10, 12, 14, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent US patent No. 6,049,565 ("Paradine et al.") in view of US patent No. 5,327,391 ("Hirata").

Regarding claims 1, 5, 12, 14, and 19, Paradine et al. teach an audio communication method and apparatus over network traffic (See Fig. 1) comprising of

an audio input (305),

an audio output (340),

interface circuitry comprising first and second jitter buffers (320 double buffer) operably coupling the audio input (305) to a voice encoder DSP (315) and third and

fourth jitter buffers (330 double buffer) operably coupling the audio output (340) to a voice decoder DSP (315),

wherein the first or second jitter buffers (320 double buffer for audio IN path) alternately fill at a first clock frequency (sampling clock via 305 CODEC circuitry block) and empty at a second clock frequency (clock on DSP side for network interface) (see Col. 4, lines 27-50),

wherein alternation between the first and second jitter buffers occurs at the second clock frequency (CCITT G.711 format 8 ms frame for DSP/network interface, See Col. 5, lines 55-65), and

wherein the third or fourth jitter buffers (330 double buffer for audio OUT path) alternately fill at the second clock frequency (clock on DSP side for network interface) and empty at the first clock frequency (sampling clock via 305 CODEC circuitry block), wherein alternation between the third and fourth jitter buffers (330 double buffer) occurs at the second clock frequency (CCITT G.711 8 ms format frame for DSP/network interface, See Col. 5, lines 55-65).

Paradine et al. teaches substantially all the claimed invention but did not disclose expressly the detailed structure of the double buffers besides their functionality and application.

Hirata teaches that the rate adaptation and jitter smoothing method with the double buffer structure comprising of

providing first circuitry (21, 25-1 and 25-2) in a first clock (101) domain operable at a first clock (101) frequency,

providing second circuitry (22, 26-1 and 26-2) in a second clock (103) domain operable at a second clock (103) frequency,

providing first and second jitter buffers (24-1 and 24-2) interfacing between the first circuitry (11) and the second circuitry (12) domain,

wherein the first or second jitter buffers (24-1 and 24-2) alternately fill at the first clock (101) frequency and empty at the second clock (103) frequency,

wherein alternation between the first and second jitter buffers (24-1 and 24-2) occurs at the second clocking frequency (104) (See Fig. 1, Col 4, lines 4-49).

A person of ordinary skill in the art would have been motivated to employ Hirata in Paradine et al. in order to obtain a method to manage double buffers across two different clock domains for transmission of voice over network and to take advantage of utilizing double buffers across different clock domains in claims 1, 5, 12, 14, and 19.

The suggestion/motivation to do so would have been to utilize double buffers across different clock domains, as suggested by Hirata in Col 4, lines 4-49. At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Hirata with the Paradine et al. to obtain the inventions specified in claims 1, 5, 12, 14, and 19.

Regarding claims 2 and 16, these claims have similar limitation as claim 1 and Paradine et al. further teach that the first circuitry comprising an audio input (305 microphone), the second circuitry comprising an encoder (315 DSP1) (See Fig. 7), thus it is rejected with the same rationale applied against claim 1 above.

Regarding claims 3 and 17, these claims have similar limitation as claim 1 and Paradine et al. further teach that the first circuitry comprising an audio input (340 speaker), the second circuitry comprising an decoder (315 DSP2) (See Fig. 7), thus it is rejected with the same rationale applied against claim 1 above.

Regarding claim 6, these claims have similar limitation as claim 1 and Paradine et al. further teach that the interface circuitry comprising one or more digital signal processors (DSP) (See Col. 4, lines 43-50), thus it is rejected with the same rationale applied against claim 1 above.

Regarding claims 4, 7-8 and 18, these claims have similar limitation as claims 1, 6 and 17 and Paradine et al. further teach that the first clock frequency comprising an audio 44.1 Khz sample clock (see Col. 4, lines 27-50), and the second clock frequency comprising a G711 compatible 8 ms frame clock (See Col. 5, lines 55-65), thus it is rejected with the same rationale applied against claims 1, 6 and 17 above.

Regarding claims 9-10, these claims have similar limitation as claim 8 and Paradine et al. further teach that that the encoded voice data may be G711 compatible 8 ms frame based as 64 samples (See Col. 5, lines 55-65), it is equivalent to a 20 ms frame with 160 samples plus buffering for overflow as 165 samples per frame (See Col. 6, lines 46-50), thus it is rejected with the same rationale applied against claim 8 above.

Regarding claim 20, this claim has similar limitation as claim 19 and Paradine et al. further teach that the encoded voice data may be transmitted based on CCITT G.711 format as 8 ms frame per voice data block, this is applicable to different frame sizes

voice codec such as GSM phone (See col. 6, lines 56-65), thus it is rejected with the same rationale applied against claim 19 above.

Response to Argument

4. The following comments fully address applicant's argument with respect to the rejection.

-- Applicant appears to argue that the cited references ("Paradine et al.") fail to show the limitation of swapping of double buffers. In response to Applicant's piecemeal analysis of the references, one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references. It is common practice in digital voice communication to separate the network interface and voice sampling by double buffering in a ping-pong style in order to adapt the interface rate difference in voice sampling (i.e. 44.1 KHz) and network interfacing (i.e. 8 KHz). Paradine et al. teaches a structure of audio input/output coupled to encoder/decoder utilizing Double Buffer structure wherein the CODEC C next to A/D (300) and D/A (335) can be viewed as a combined audio input/output sampling unit. It is common practice that in voice/audio digitization application, the voice input is sampled via "CODEC" unit which performs analog sample holding, filtering, and conversion (Coding) and vice versa (Decoding). Thus the term CODEC is often interchanged for voice/audio sampling unit. Thus, it is reasonable to combined CODEC C with A/D (300) and D/A (335) as voice/audio sampling block. Industrial Codec Chips such as Texas Instrument's TCM129C16 is an examples. Furthermore, the DSP (315) transforms samples from the

double buffer (320) from 16 bits at 44.1 Khz format into a new digital format with 8 Khz, 8-bit mu-law samples and vice versa. Thus the DSP (315) perform the Coding and Decoding functions between two digital streams with different sampling rate and code format. Thus, it is reasonable to view the DSP (315) including voice encoder and decoder functions. The rejections are based on combinations of Paradine et al. in view of Hirata wherein Hirata further teaches the swapping of double buffers using a double buffer structure.

-- Applicant also appears to argue that the cited references ("Hirata") fails to disclose the limitation of switching individual ones of pairs of buffers according to a same frequency. Hirata further teaches a common operation of "double buffers" with separate write-in and read-out within separate clock/frame domains (reception clock/frame as first clock/frame domain and system clock/frame as second clock/frame domain), wherein the first or second jitter buffers (24-1 and 24-2) alternately (by circuit 21) fill (write-in) at a first clock frequency (connected to 101 for WRITE-IN) (See Fig. 1, Cool. 4, lines 15-24) and empty (read-out) at a second clock frequency (connected to 103 for READ), wherein the alternation (by 22) between the first and second jitter buffers (24-1 and 24-2) occurs at the second clock frequency (connected to 103) (See Fig. 1, Cool. 4, lines 36-49). The double buffers (24-1 and 24-2) are applied as the first and second buffers in one direction (Read as audio in direction wherein second clock connected to output and first clock connected to input) and also as the third and fourth buffers (24-1 and 24-2) in the reverse direction (Read as audio out direction wherein second clock connected to input and first clock connected to output) wherein the third or

fourth jitter buffers (24-1 and 24-2 in reverse direction) alternately (by 21) fill (write-in) at the second clock frequency (connected to 101 for WRITE-IN) (See Fig. 1, Cool. 4, lines 15-24) and empty (read-out) at the first clock frequency (connected to 103) (See Fig. 1, Col. 4, lines 36-49), wherein alternation (by 22) between the third and fourth jitter buffers (24-1 and 24-2 in reverse direction) occurs at the second clock frequency (connected to 101) (See Fig. 1, Col. 4, lines 15-24). Furthermore, either side can control the buffers alternating.

As such, Hirata teaches the limitation of switching individual ones of pairs of buffers according to a same frequency.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chang whose telephone number is (571) 272-3129. The examiner can normally be reached on Monday - Friday from 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

rkc

Richard Chang
Patent Examiner
Art Unit 2616

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER